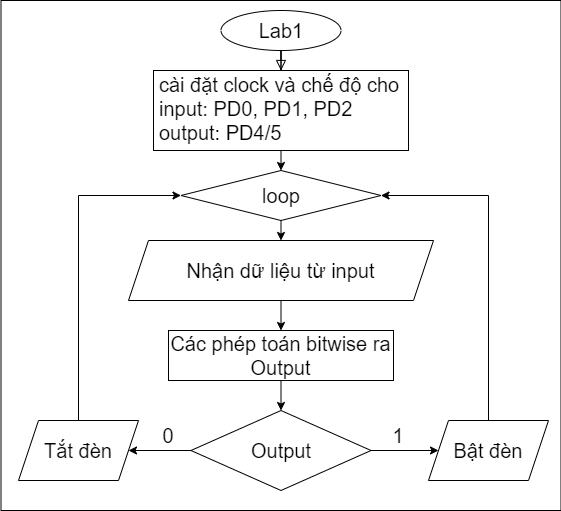
Lab 1 Report

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# Flowchart



# Code

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* main.s \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

; Program initially written by: Yerraballi and Valvano

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; Date Created: 1/15/2018

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; Brief description of the program: Solution to Lab1

; The objective of this system is to implement a parity system

; Hardware connections:

; One output is positive logic, 1 turns on the LED, 0 turns off the LED

; Three inputs are positive logic, meaning switch not pressed is 0, pressed is 1

GPIO\_PORTD\_DATA\_R EQU 0x400073FC

GPIO\_PORTD\_DIR\_R EQU 0x40007400

GPIO\_PORTD\_DEN\_R EQU 0x4000751C

GPIO\_PORTE\_DATA\_R EQU 0x400243FC

GPIO\_PORTE\_DIR\_R EQU 0x40024400

GPIO\_PORTE\_DEN\_R EQU 0x4002451C

SYSCTL\_RCGCGPIO\_R EQU 0x400FE608

PRESERVE8

AREA Data, ALIGN=2

; Declare global variables here if needed

; with the SPACE assembly directive

ALIGN 4

AREA |.text|, CODE, READONLY, ALIGN=2

THUMB

EXPORT EID

EID DCB "213731",0 ;replace ABC123 with your EID

;sw PD2, PD1, PD0 and led on PD4

EXPORT RunGrader

ALIGN 4

RunGrader DCD 1 ; change to nonzero when ready for grading

EXPORT Lab1

Lab1

;Enable clock for port D

MOV R0,#0x08

LDR R1,=SYSCTL\_RCGCGPIO\_R

STR R0,[R1]

NOP

NOP

;Config D0,1,2 for input, D4 for output

LDR R1,=GPIO\_PORTD\_DIR\_R

MOV R0,#0x10 ;10000

STR R0,[R1]

;Enable data pin of PD

LDR R3,=GPIO\_PORTD\_DEN\_R

MOV R2,#0x17

STR R2,[R3]

;Set R3 as PD\_DATA for futher used

LDR R3,=GPIO\_PORTD\_DATA\_R

loop

;Y = D0 ^ D1 ^ D2

LDR R4,[R3]

NOP

NOP

AND R5,R4,#0x00000001 ;D0 = R5

AND R6,R4,#0x00000002 ;D1 = R5

AND R7,R4,#0x00000004 ;D2 = R7

;Have to shift bits before compare them

LSR R6,R6,#1

LSR R7,R7,#2

EOR R5,R5,R6

EOR R5,R5,R7 ;Y = R5

MOV32 R6,#0x00000001

BIC R5,R6,R5

LSL R5,R5,#4 ;shift left 4 is pd4

STR R5,[R3]

B loop

ALIGN ; make sure the end of this section is aligned

END ; end of file

# Result

